IN THE CLAIMS

Please amend the claims as follows:

1. - 28. (Canceled)

29. (Currently Amended) A voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node and a second split-level input node, the second split-level input node directly coupled to an output of the inverter, and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node;

wherein the static voltage-level converter includes two down-sized transistors.

30. (Previously Presented) The voltage-level converter of claim 29, wherein the two down-sized transistors are insulated gate field-effect transistors.

31. (Currently Amended) A voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node and a second split-level input node, the second split-level input node directly coupled to an output of the inverter, and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node;

wherein the static voltage-level converter comprises:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node; and

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node, wherein the inverter is coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are down-sized.

32. (Previously Presented) The voltage level converter of claim 31, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are insulated gate field-effect transistors.

33. (New) The voltage-level converter of claim 29, wherein the static voltage-level converter includes an input node adapted to receive an input signal, the input signal including a first pair of signal levels.

34. (New) The voltage-level converter of claim 33, wherein the static voltage-level converter further includes a first output node adapted to generate a first output signal including a second pair of signal levels.

35. (New) The voltage-level converter of claim 34, wherein the static voltage-level converter further includes a second output node adapted to generate a second output signal including the second pair of signal levels, the second output signal being the complementary signal of the first output signal.

36. (New) The voltage-level convert of claim 35, wherein the second pair of signal levels includes at least one voltage signal level that is a greater than any voltage signal level in the first pair of signal levels.

37. (New) The voltage-level converter of claim 31, wherein the split-level output circuit includes a split-level output node, a first insulated-gate field-effect transistor (FET) coupled to the first split-level input node and a second insulated-gate FET coupled to the second split-level input node, the first insulated-gate FET being connected in series with the second insulated-gate FET, the first insulated gate FET and the second insulated gate FET having a common node coupled to the split-level output node and the first split-level input node coupled to the first output node of the static voltage-level converter, and the second split-level input node coupled to the second output node of the static voltage-level converter.

38. (New) The voltage-level converter of claim 37, wherein the first output node of the static voltage-level converter is directly coupled to the first split-level input node of the split-level output circuit, and the second output node of the static voltage-level converter is directly coupled to the second split-level input node of the split-level output circuit.

39. (New) The voltage-level converter of claim 37, wherein the first insulated-gate field-effect transistor of the split-level output circuit comprises a p-type insulated-gate field-effect transistor.

40. (New) The voltage-level converter of claim 37, wherein the second insulated-gate field-effect transistor of the split-level output circuit comprises an n-type insulated gate field-effect transistor.

41. (New) A logic unit comprising:

one or more first logic units adapted to operate at a first voltage;

one or more second logic units adapted to operate at a second voltage, the second voltage being greater than the first voltage; and

a voltage-level converter coupling at least one of the one or more first logic units to at least one of the one or more second logic units, the voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node and a second split-level input node, the second split-level input node directly coupled to an output of the inverter, and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node;

wherein the static voltage-level converter includes two down-sized transistors.

42. (New) The logic unit of claim 41, wherein the static voltage-level converter includes:

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to an input node coupling the static voltage-level converter to the one or more first logic units.

43. (New) The logic unit of claim 42, wherein the static voltage-level converter further includes:

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to a first output node.

44. (New) The logic unit of claim 43, wherein the inverter is coupled to the input node and to a second output node of the static voltage-level converter.

45. (New) The logic unit of claim 44, wherein the first output node of the static voltage-level converter is directly coupled to the first split-level node of the split-level output circuit, and the second output node of the static voltage-level converter is directly coupled to the second split-level node of the split-level output circuit.

46. (New) The logic unit of claim 41, wherein the split-level output circuit comprises a plurality of insulated-gate field-effect transistors.

47. (New) The logic unit of claim 46, wherein the split-level output circuit includes no more than two insulated-gate field effect transistors.

48. (New) A system comprising:

A first logic unit coupled to a first node, the first node powered at a first voltage level;

a second logic unit coupled to a second node, the second node powered at a second voltage level that is greater than the first voltage level;

a voltage level converter coupling the first logic unit and the second logic unit, the voltage level converter adapted to convert logic signals produced by the first logic unit to logic signals compatible with the second logic unit;

wherein the voltage level converter includes:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node and a second split-level input node, the second split-level input node directly coupled to an output of the inverter, and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node;

wherein the static voltage-level converter includes two down-sized transistors.

49. (New) The system of claim 48, wherein the first logical unit is a non-critical functional unit.

50. (New) The system of claim 49, wherein the non-critical function unit is a memory.

51. (New) The system of claim 48, wherein the second logical unit is a critical functional unit.

52. (New) The system of claim 51, wherein the critical function unit is a clock generation circuit.

53. (New) The system of claim 48, wherein the first logic unit includes one or more logic units in a non-critical path, and the second logic unit includes one or more logic units in a critical path.

54. (New) A system comprising:

a communication unit;

a logic unit embedded in the communication unit; the logic unit including:

one or more first logic units adapted to operate at a first voltage;

one or more second logic units adapted to operate at a second voltage, the second voltage being greater than the first voltage; and

a voltage-level converter for coupling at least one of the one or more first logic units to at least one of the one or more second logic units, the voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, the split-level output circuit including a first split-level input node and a second split-level input node, the second split-level input node directly coupled to an output of the inverter, and the first split-level input node adapted to receive a complementary signal of the signal received at the second split-level input node;

wherein the static voltage-level converter includes two down-sized transistors.

55. (New) The system of claim 54, wherein the static voltage-level converter further includes:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node;

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node; and

an inverter coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

56. (New) The system of claim 54, wherein the communication unit is a cell phone.